

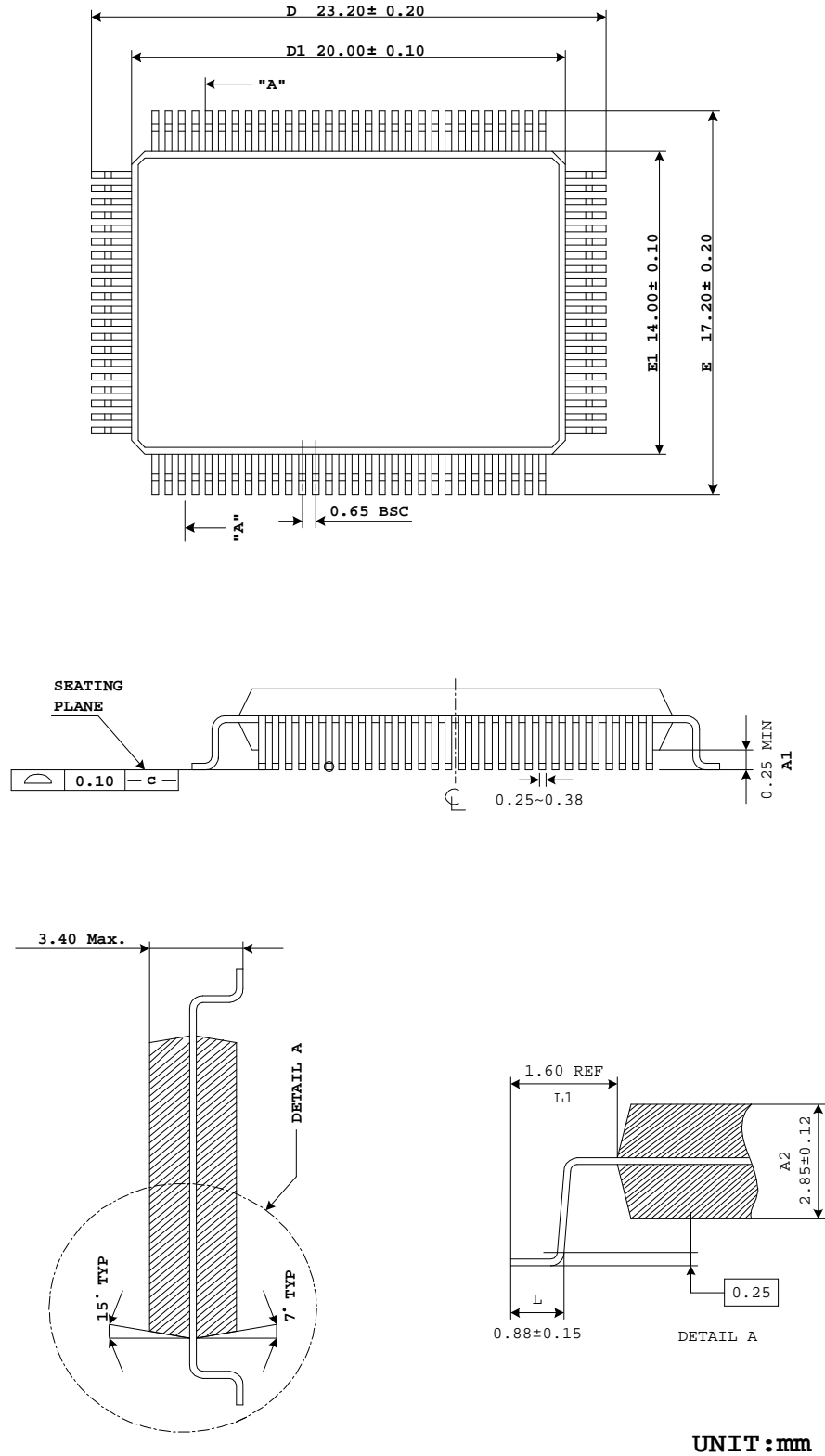
R8830I
Brief Sheet
16-BIT RISC MICROCONTROLLER

1. Features

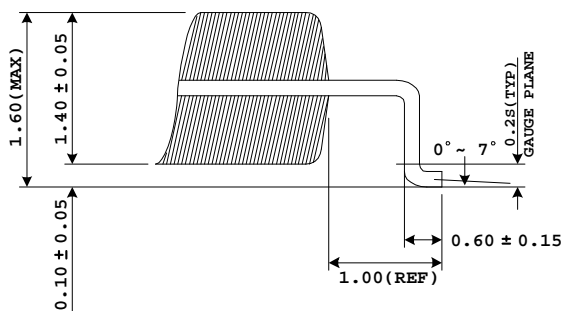
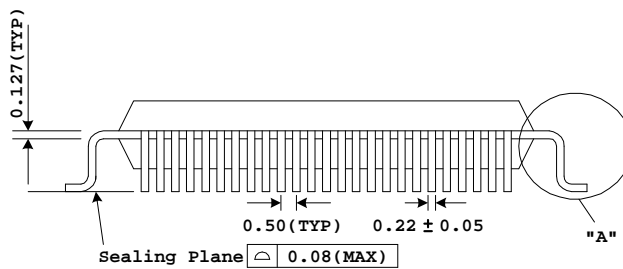
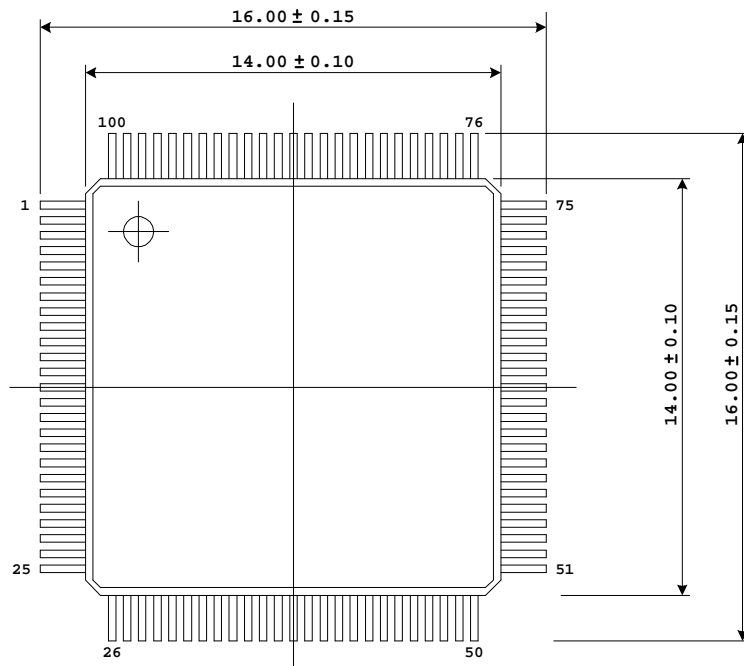
- **CPU Core**
 - RDC's proprietary RISC architecture
 - Five-stage pipeline
 - CPU Clock : 25 MHz
 - Supports CPU ID
 - Supports 32 PIO pins
- **Bus interface**
 - Multiplexed address and data bus which is compatible with the 80C188 microprocessor
 - Supports a non-multiplexed address bus A[19:0]
- **ROM/RAM Controller and Addressing Space**
 - 1M-byte memory address space
 - 64K-byte I/O space
- **PSRAM Interface**
 - PSRAM (Pseudo Static RAM) interface with auto-refresh control
- **Compatible UART Channels**
 - UART speed : maximum baud rate up to 115.2Kbps
- **Two Independent DMA Channels**
 - Supports serial ports with DMA transfers
- **Asynchronous Serial Channels**
 - Supports two asynchronous serial channels with hardware handshaking signals
- **Interrupt Controller**
 - The Interrupt controller with seven maskable external interrupts and one non-maskable external interrupt
- **Programmable Chip-select Logic**
 - Programmable chip-select logic for memory or I/O bus cycle decoder
- **Programmable Wait-state Generator**
- **Counter/Timers**
 - Three independent 16-bit timers and one independent watchdog timer
- **Software Compatible with the 80C186 Microprocessor**
- **Operating Voltage Range**
 - Core voltage: 5V ± 10%
 - I/O voltage: 5V ± 10%
- **Ambient temperature: - 40 ~ +85°C**
- **Power Save and Power Down Mode Support**
- **Package Type**
 - 100 Pin PQFP & 100 Pin LQFP

3. Package Information

PQFP 100 pins



LQFP 100 pins



UNIT : mm