

R3210
Brief Sheet
FAST ETHERNET RISC PROCESSOR

1. Features

n Embedded RISC Controller

- Full 32 bit RISC architecture
- Supports diverse operation systems, including Windows based, Linux and most popular 32 bit RTOS
- 6 stage pipeline
- Operation frequency: 133 MHz
- Supports MMU function which includes 32 TLB entries

n On Chip L1 16KB Cache

- Unifies instructions and data cache
- Supports write through for cache write policy
- Snooping mechanism support for data coherence between main memory and cache
- Direct map

n SDRAM Control Interface

- PC100/ PC133 compliant
- Supports 16-bit data bus width
- Supports speeds up to 133 MHz and above
- Supports maximum 128 Mbyte memory space

n X-Bus Interface

- Provides the interface to boot ROM BIOS & DOC (Disk On Chip).
- Supports 8/16 bit data width
- Provides ROMCS_n for booting from X-bus Flash ROM
- Supports from 64Kbyte to Max. 16Mbyte ROM space addressing
- Supports two independent and programmable CSs (Chip Selects)

n LPC (Low Pin Count) Bus Interface

- LPC revision 1.0 compliant
- Supports LPC/ FWH (Firmware Hub) compliant interfaces
- Provides the interface to connect an LPC/FWH Flash ROM or Super I/O chip
- Supports LPC DMA
- Supports serial IRQ
- Supports bus master mode

n MAC Controller

- Supports two-port 10/100 Fast Ethernet MAC
- IEEE 802.3u MII interface
- IEEE 802.3x flow control in full-duplex mode
- Descriptor architecture for packet TX/RX

n PCI Control Interface

- Supports PCI Rev 2.1 specification
- 32-bit bus interface
- Supports PCI clock at 33 MHz
- Supports PCI host
- Supports PCI master / slave
- Up to 133 Mbytes / sec maximum bandwidth
- Supports up to 3 external master devices on PCI
- Provides four PCI interrupt channels

n DMA Controller

- Provides two 8237 DMA compatible controllers which are cascaded internally
- 4 channels for 8 bit DMA transfer and 3 channels for 16 bit transfer
- Supports 8/ 16 / 32-bit channel 4 bus masters on the LPC bus

n Interrupt Controller

- Provides two 8259 compatible interrupt controllers which are cascaded internally
- Independent programmable level/ edge-triggered interrupt channels
- Serial IRQ supported

n Counter / Timers

- 8254 compatible timers
- Provides three independent programmable timers / counters
- Supports a watchdog timer (WDT)
- Supports a speaker output

n Real Time Clock (External)

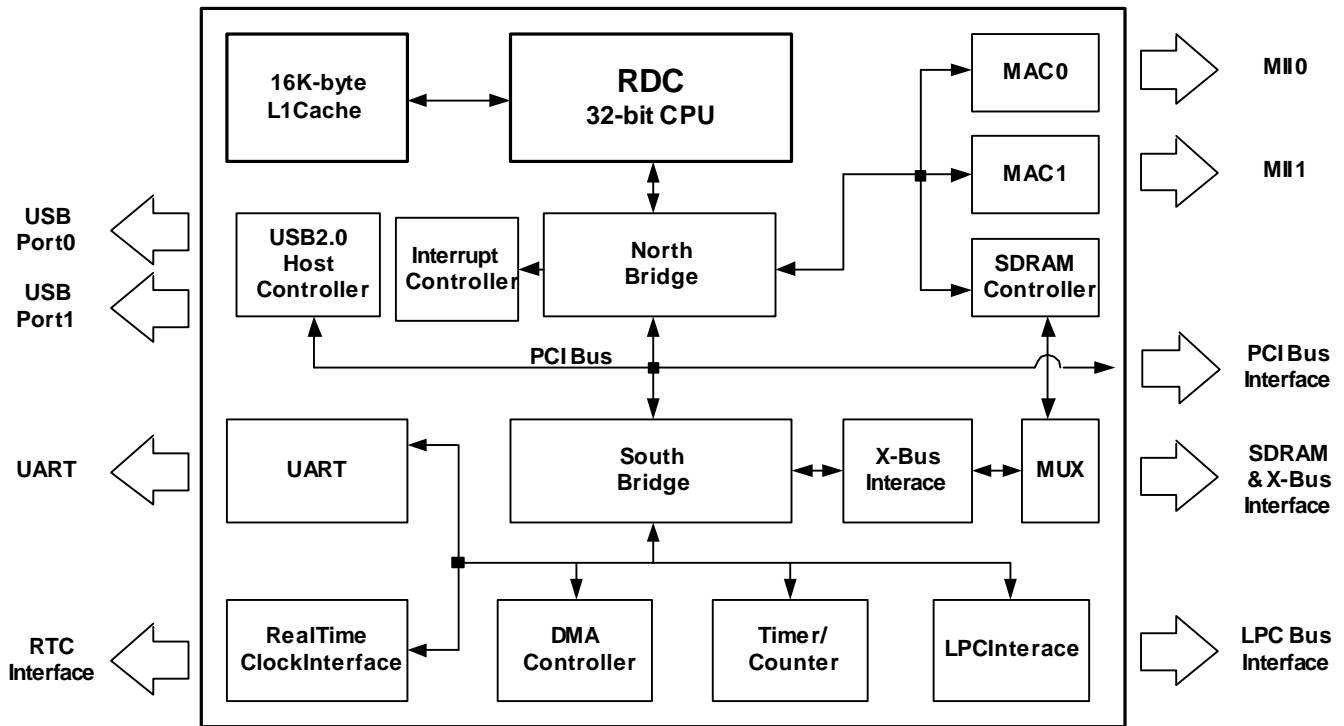
- Provides a direct interface to external RTC chips

n FIFO UART Port

- A high performance UART port with transmit and receive FIFOs

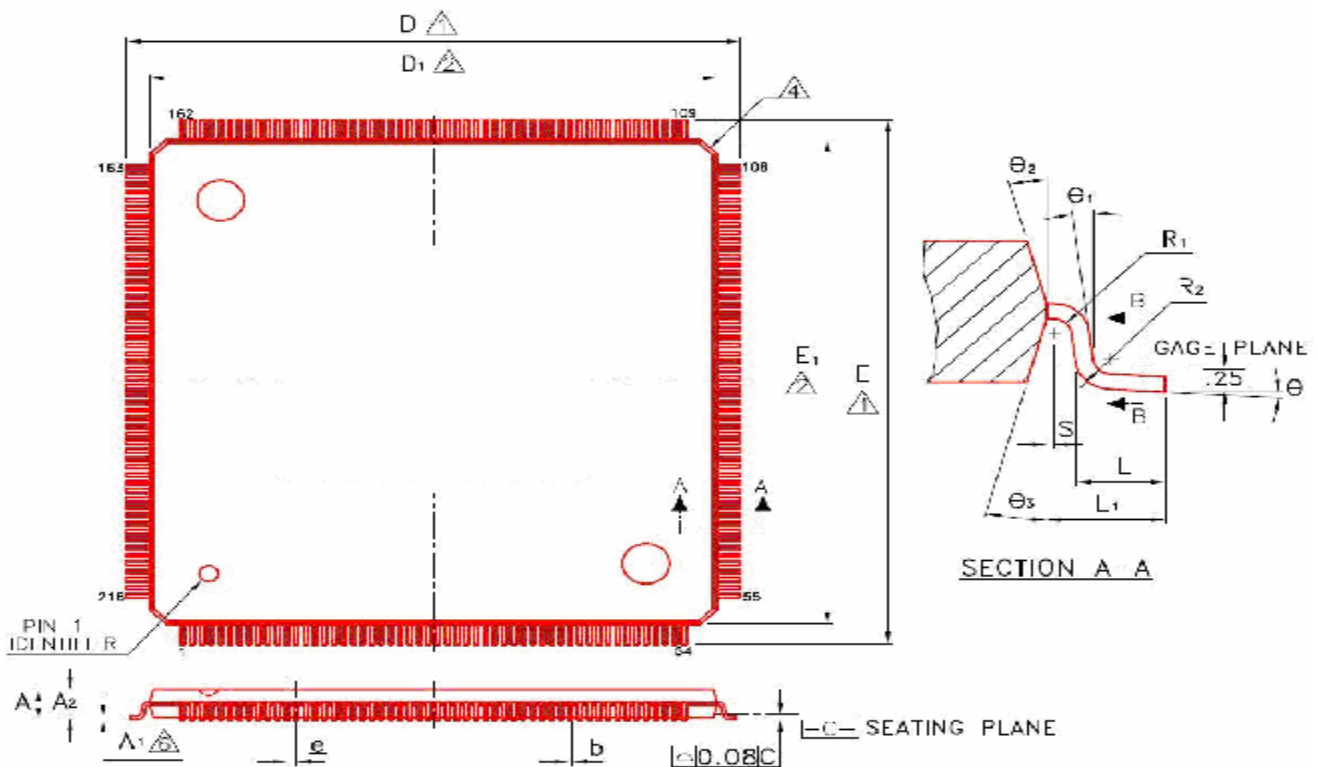
- Supports the programmable baud rate generator with the data rates from 50 to 115,200 bps
- The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
- n **General Programmable I/ O**
 - Supports 58 programmable I/O pins
 - Each GPIO pin can be individually configured to be an input/output pin
- n **Operating Voltage Range**
 - Core voltage : 1.8 V \pm 5%
 - I/ O voltage : 3.3 V \pm 10%
- n **Two USB 2.0 Host Port Support**
 - Supports HS, FS and LS
- n With 216 Pin LQFP & LFBGA-225 package type
- n A green product

2. Block Diagram



3. Package Information

LQFP 216 pins



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	--	--	1.60
A ₁	0.05	--	0.15
A ₂	1.35	1.40	1.45
b	0.13	0.18	0.23
D	25.85	26.00	26.15
D ₁	23.90	24.00	24.10
E	25.85	26.00	26.15
E ₁	23.90	24.00	24.10
e	0.40 BSC		
L	0.45	0.60	0.75
L ₁	1.00 REF		
R ₁	0.08	--	--
R ₂	0.08	--	--
S	0.20	--	--
Θ	0°	3.5°	7°
Θ ₁	0°	--	--
Θ ₂	11°	12°	13°
Θ ₃	11°	12°	13°

LFBGA 225 balls

