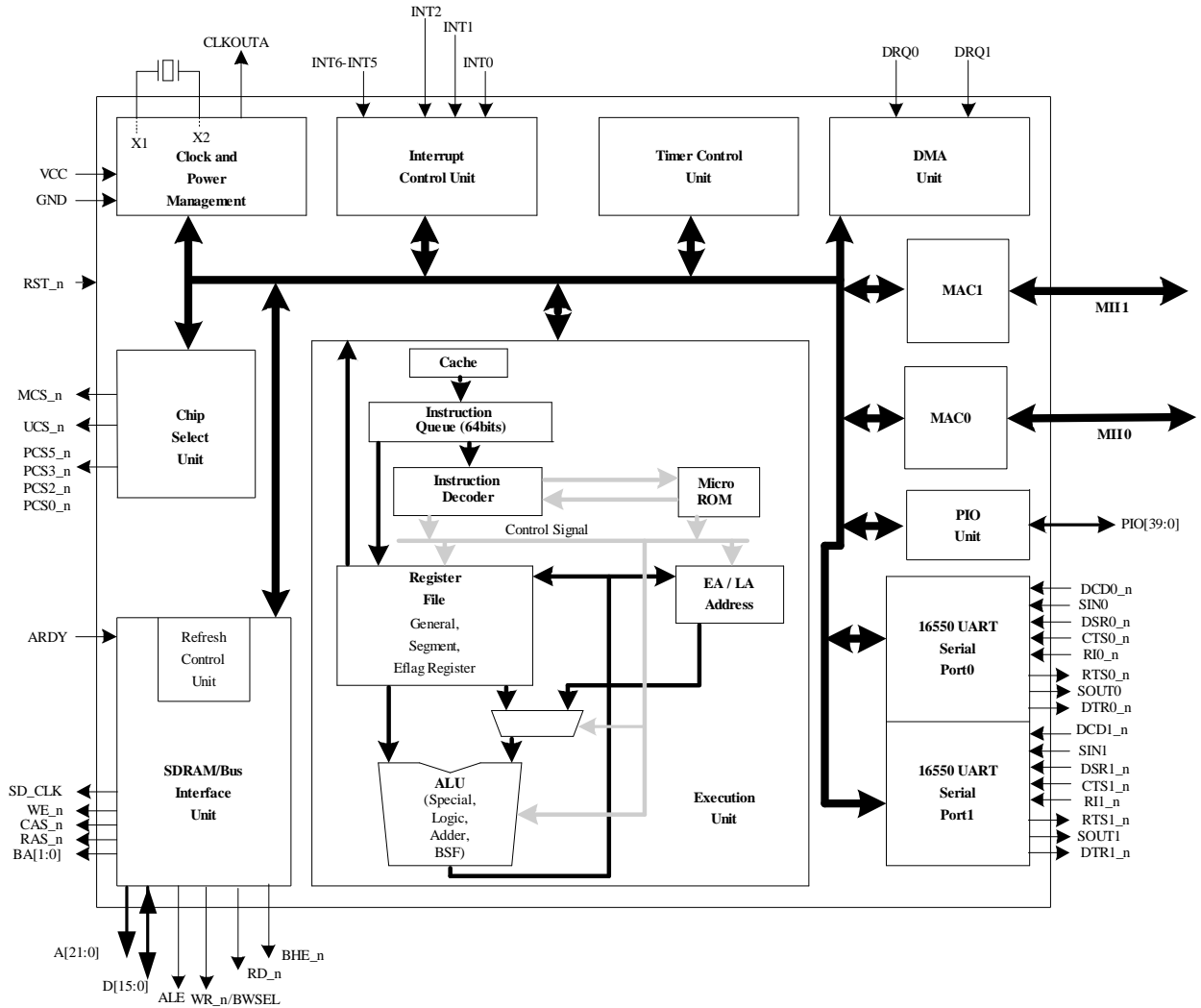


R2022
Brief Sheet
FAST ETHERNET RISC PROCESSOR

1. Features

- | Five-stage pipeline
- | RISC architecture
- | Bus interface
 - 16-bit data bus [15:0]
 - Supports a non-multiplexed address bus A[21:0]
 - 8-bit or 16-bit external bus dynamic access
 - 16M-byte memory address space Address [23:0]
 - 64K-byte I/O space
 - Supports an independent data/address bus for external I/O devices
- | Supports two compatible UART serial channels with 16-byte FIFOs and hardware flow-control
- | Supports CPU ID
- | Supports a glueless and simplified 16-bit PCMCIA bus interface
- | Supports 40 PIO pins
- ≠ SDRAM control interface
- | Three independent 16-bit timers and one independent programmable watchdog timer
- | The interrupt controller with five maskable external interrupts and one non-maskable external interrupt
- | Two independent DMA channels
- | Programmable chip-select logic for memory or I/O bus cycle decoder
- | Programmable wait-state generators
- | With 8-bit or 16-bit boot ROM bus size
- | 2-port Fast Ethernet MAC with MII interface
- | Supports an 8K-byte uniform cache
- | The MAC packet buffer is cacheable with snooping function
- | With 25MHz input frequency and up to 125 MHz maximum internal frequency
- | Compatible with 3.3V I/O and 2.5V core voltage
- | Package type includes 128-pin PQFP

2. Block Diagram



3. Package Information

PQFP 128 pins

