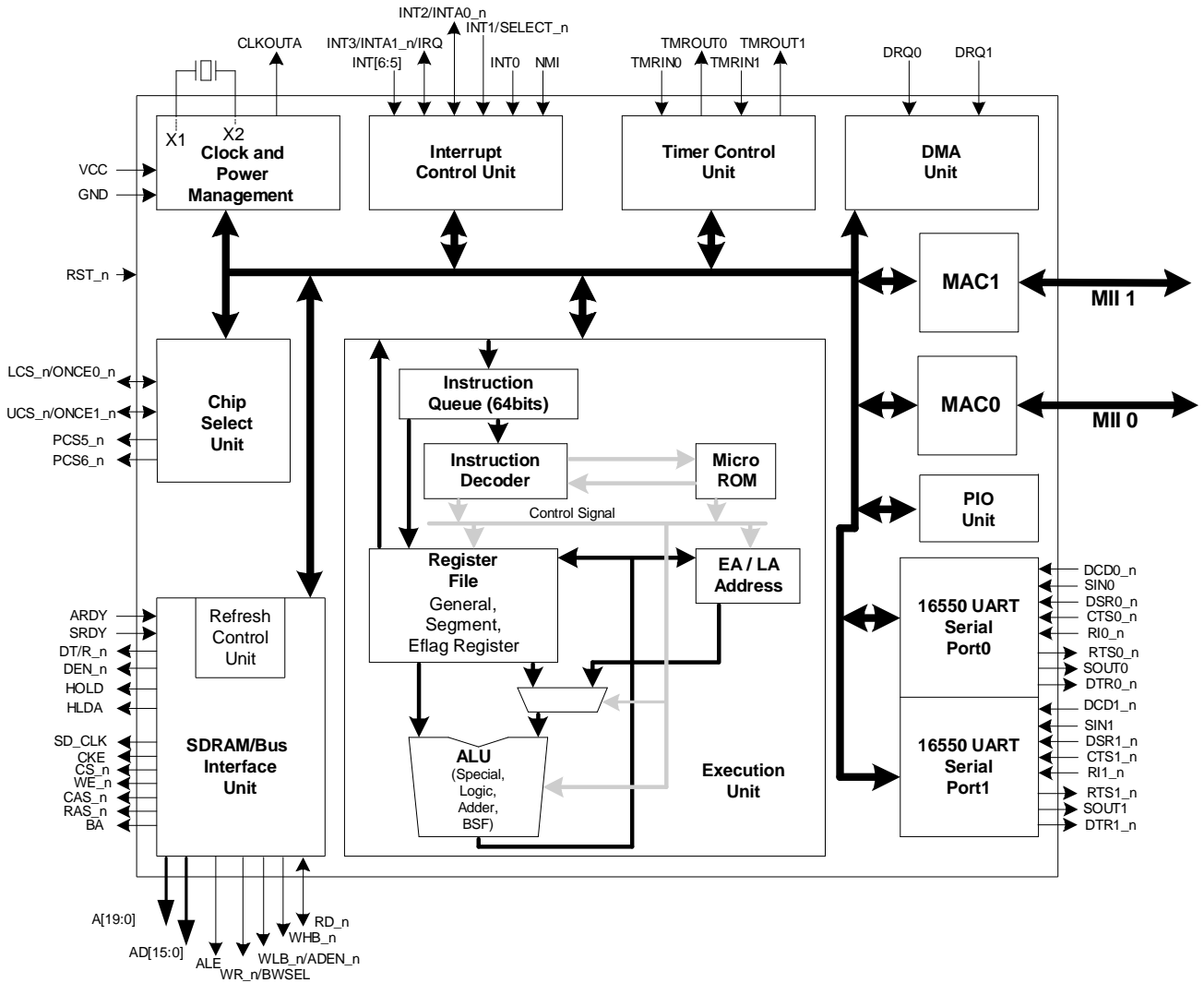


**R1620**  
**Brief Sheet**  
**FAST ETHERNET RISC PROCESSOR**

## **1. Features**

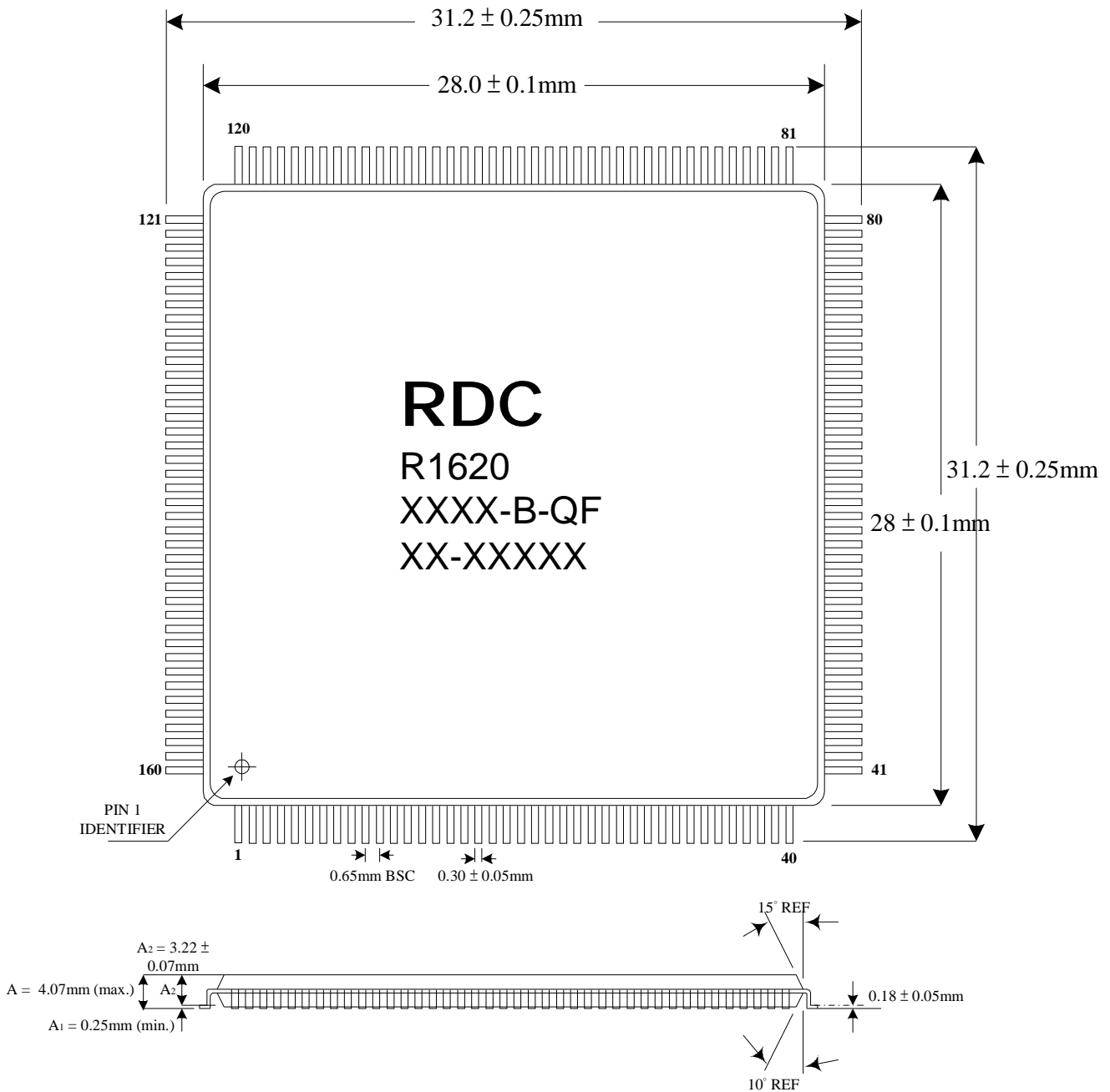
- I Five-stage pipeline**
- I RISC architecture**
- I Bus interface**
  - Multiplexed address and Data bus
  - Supports non-multiplexed address bus A[19:0]
  - 8-bit or 16-bit external bus dynamic access
  - 1M-byte memory address space
  - 64K-byte I/O space
  - Supports an independent bus for slower I/O device
- I Software is compatible with the 80C186 microprocessor**
- I Supports two 16550 UART serial channel with 16 bytes FIFO.**
- I Supports CPU ID**
- I Supports 32 PIO pins**
- I SDRAM control Interface**
- I Three independent 16-bit timers and one independent programmable watchdog timer**
- I The Interrupt controller with six maskable external interrupts and two non-maskable external interrupt**
- I Two independent DMA channels**
- I Programmable chip-select logic for Memory or I/O bus cycle decoder**
- I Programmable wait-state generator**
- I With 8-bit or 16-bit Boot ROM bus size**
- I 2-Port Fast Ethernet MAC with MII interface**
- I With 25MHz input frequency and up to 4x25MHz maximum internal frequency.**
- I Compatible with 3.3V I/O.**
- I Package Types include 160-pin PQFP and 160-pin LQFP.**

2. Block Diagram



3. Package Information

PQFP 160 pins



**LQFP 160 pins**

