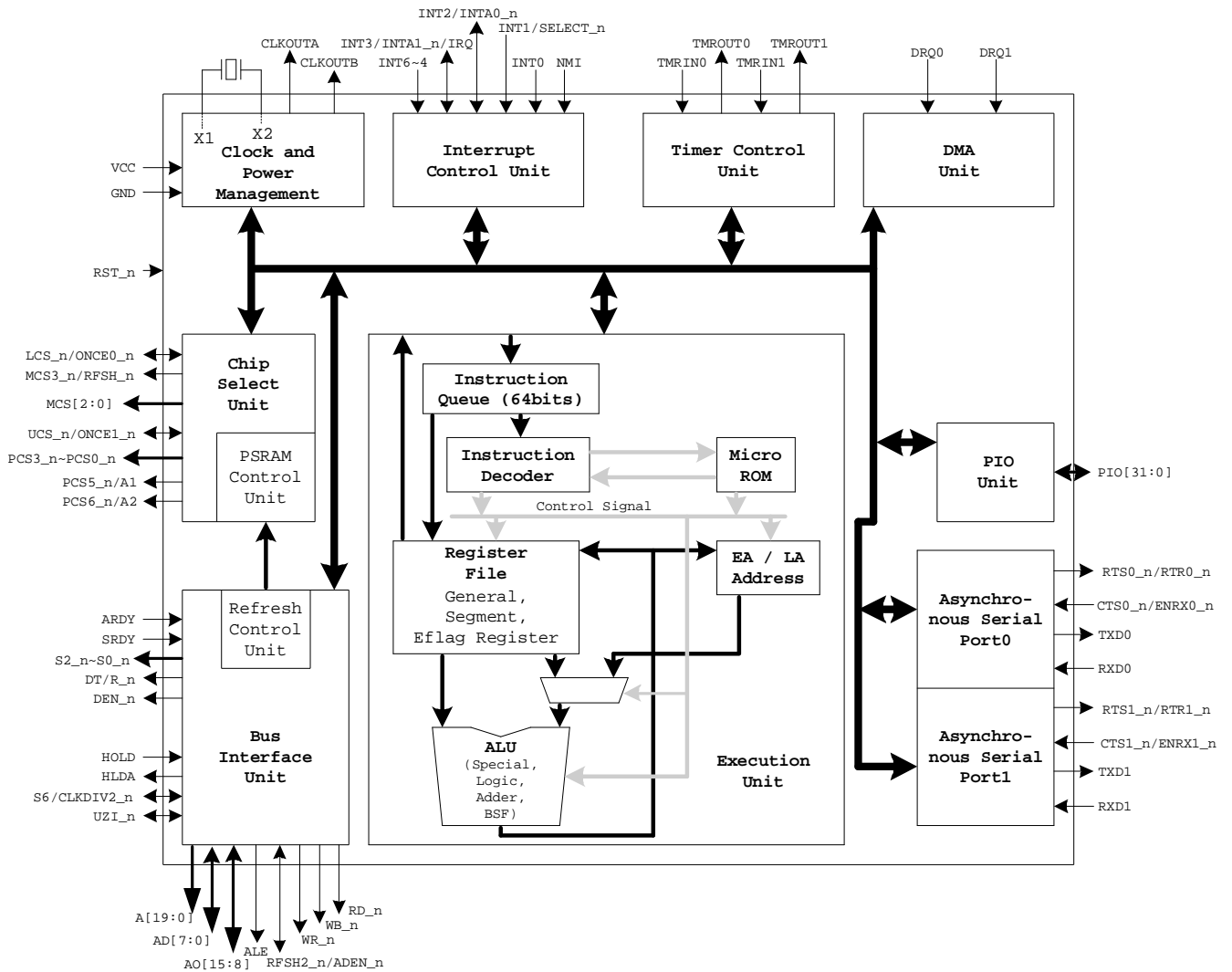


**R1120**  
**Brief Sheet**  
**16-BIT RISC MICROCONTROLLER**

## 1. Features

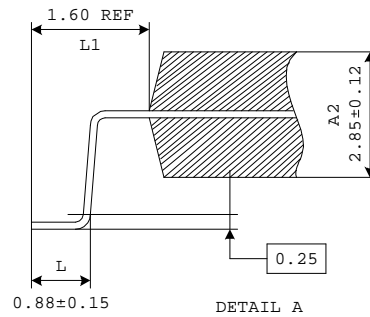
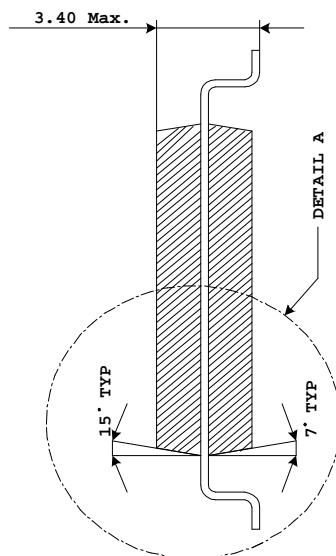
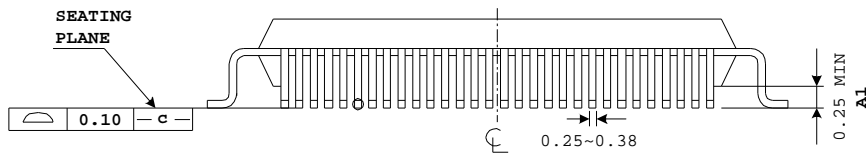
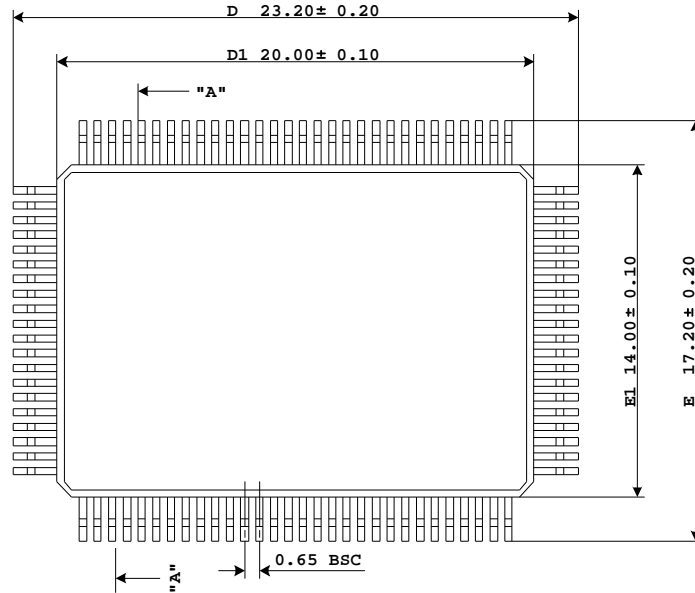
- | Five-stage pipeline
- | RISC architecture
- | Integrated PLL (\*1~\*8)
- | Maximum frequency: 80 MHz; the external bus, internal bus and core are operating in the same clock base
- | Static & synthesizable design
- | Bus interface
  - A multiplexed address and data bus which is compatible with the 80C186 microprocessor
  - Supports a direct address bus A[19:0]
  - 1M-byte memory address space
  - 64K-byte I/O space
- | Software is compatible with the 80C186 microprocessor
- | Supports two asynchronous serial channels with hardware handshaking signals
- | Supports CPU ID
- | Supports 32 PIO pins
- |
- |
- | PSRAM (Pseudo static RAM) interface with auto-refresh control
- | Three independent 16-bit timers and one independent watchdog timer
- | The Interrupt controller with seven maskable external interrupts and one non-maskable external interrupt
- | Two independent DMA channels
- | Programmable chip-select logic for memory or I/O bus cycle decoder
- | Programmable wait-state generators
- | The I/O pin output is 3.3 volt level and the input 3.3 to 5 volt tolerance.
- | 3.3V operation voltage
- | Supports serial port/ DMA transfers
- | With 8-bit or 16-bit boot ROM bus size
- | A green product
- | Package Type
  - PQFP100 pins & LQFP100 pins

## 2. Block Diagram



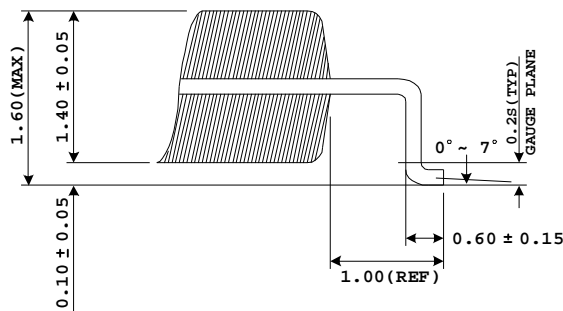
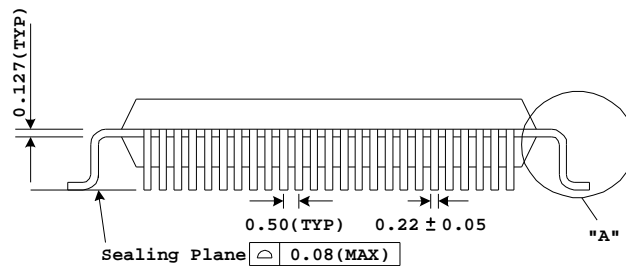
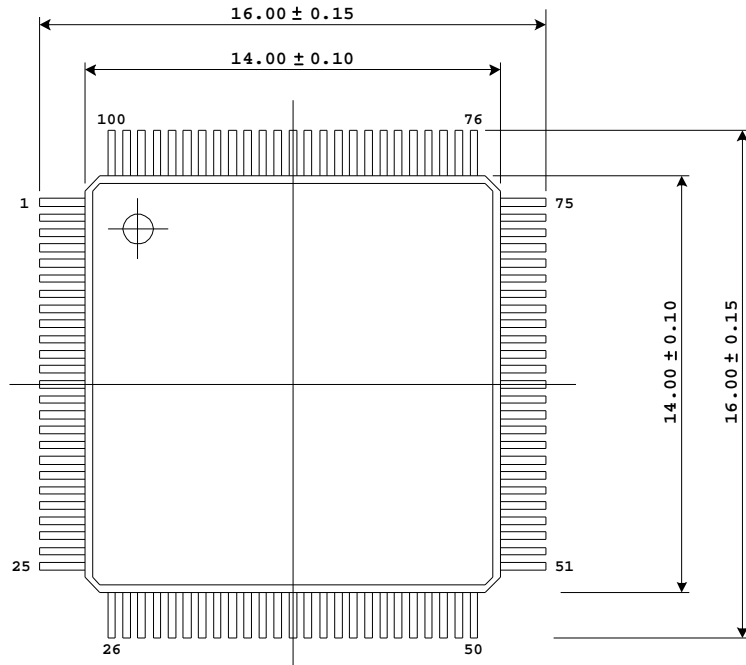
3. Package Information

PQFP100 pins



UNIT : mm

LQFP100 pins



UNIT : mm